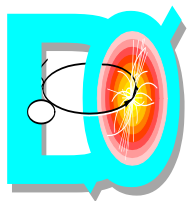


Using Multiple SVX 4 Buffers in D0

Marvin Johnson



SVX 4 controls

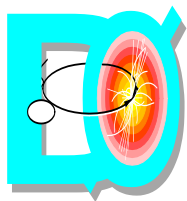
- All SVX 4 controls are the same for D0 and CDF
- Both CDF and D0 use the bi directional data register for control
 - D0 uses all 8 bits
 - CDF uses only 4
 - Other 4 bits are on separate pads
 - Used for front end control
- D0 has 4 additional lines from sequencer so full SVX 4 could be implemented
 - Impact on cable plant and interface boards
- CDF has 2 sets of clock lines



Buffers And L1 Rates

- The table below shows dead time as a function of buffer size (single queue, poisson arrival and process
- 4 buffers give a factor of 10 for 5% dead time
- 1 buffer gives a factor of 5
 - Biggest gain is from 1 buffer

Buffers	R for 10%	L1 rate at 10%	R for 5%	L1 rate at 5%
1	.11111	7,406	.0526	3,508
2	.3935	26,232	.2572	17,149
3	.6021	40,141	.4416	29,442
4	.7394	49,295	.5766	38,443
5	.8314	55,426	.6738	44,924
6	.8952	59,677	.7451	49,675
7	.94089	63,723	.7986	53,241
8	.9745	64,969	.8397	55,980



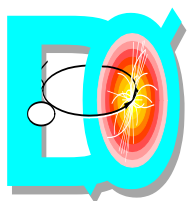
Hybrid approach

- Simple scheme to use 1 additional SVX 4 buffer
- Minimal impact on D0 infrastructure
- Works only for 396 ns operation



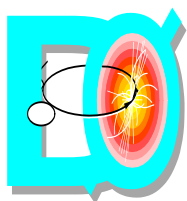
Details-clock

- Add separate front end clock
 - Looks as if it can run all the time
 - 396 ns period
 - No need for sequencer control
 - Build separate 25 to 1 fan-out cards
 - Locate these cards in the x row of adapter card ring (it is half full)
 - Need 18 cards for each half
 - Use one of these cards as a master
 - Control it with a new cad or modified sequencer controller
 - Switching back to current mode requires some thought
 - Needs cables from adapter card ring to SVX chips



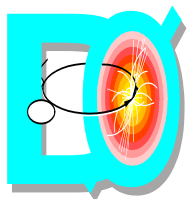
Details- Control

- Run SVX 4 in CDF mode
- At first L1 accept:
 - Switch to D0 mode.
 - Generate L1 accept and 2 PRD1 signals using the data buss
 - Switch back to CDF mode, digitize and readout
 - Front end clock continues to operate
 - D0 mode must last less than 396 ns (21 clocks). C\currently 22 clocks.
- If another L1 accept occurs before end of readout, stop the front end clock, raise front end busy.
 - Locks the data in the pipe line



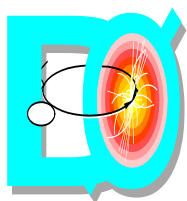
More Details

- At end of read out
 - If no pending L1, switch to D0 mode issue a PRD2 signal, switch back to CDF and continue
 - If L1 accept, switch to D0 mode, issue PRD 2, L1 A and 2 PRD1's.
 - Front end clock is stopped so no constraint on time.
 - Switch to CDF mode
 - Lower front end busy
 - Restart front end clock
 - Digitize and readout as above.
- Can't switch modes during digitize.
 - Ramp is running
- Can't switch modes during readout
 - Buss is set for readout.



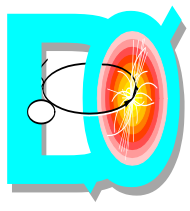
Draw backs

- Noise in Calorimeter
 - Could be quite difficult
- Project delay
 - Likely several months
- CFT system must be replaced
 - It is SVX 2 and would limit the L1 rate.



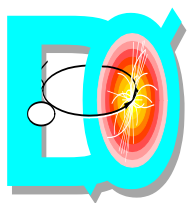
What must Change

- Use V cal line for mode control
 - Not planned for use in D0
 - Needs a jumper wire added to interface board
 - SVX hybrid needs modification
- Add new front end clock.
 - New fan out card (pretty simple)
 - Needs controller card (modified Sequencer controller?)
 - Needs new cables to junction card
 - Needs modified digital cable
 - Needs modified SVX 4 hybrid



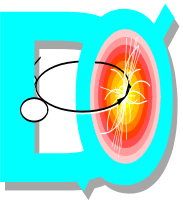
Hybrid changes

- Vcal line goes to all chips so switching it to mode control should not be difficult
- New clock lines are more difficult
 - May be hard to route
 - May need larger connector
 - 50 pin connector has 9 grounds
 - Could take 2 for clock but not my preference
 - 6 power pins so 7 grounds is safe but ground pins usually help quiet the circuit.



CFT system

- Could use existing Trip chips
 - Better to rerun them to fix small bug
 - Probably no real cost (small size)
- Replace AFE boards
 - R and D on Trip is nearly done
 - Layout can use much of existing board
 - Much simpler design
 - Minimum of 2 years.
 - Could run a mixed old and new system (slow rate) if not all finished in time



Summary

- THIS SCHEME HAS NOT BEEN TESTED
 - Test as soon as possible
- Currently have a low L1 rate
 - Extra 1-2 μs because of SVX 2 bugs
 - Can't restart pipeline because of SVX 2 bugs (4.2 μs)
 - Total time is 10 μs plus readout
 - Readout is also longer than expected (noise?)
- CDF is now at 12 KHz.
- Can get a factor of 5 with some technical and schedule risk
 - Need to understand the reasons for current high occupancy.